

Figure 1

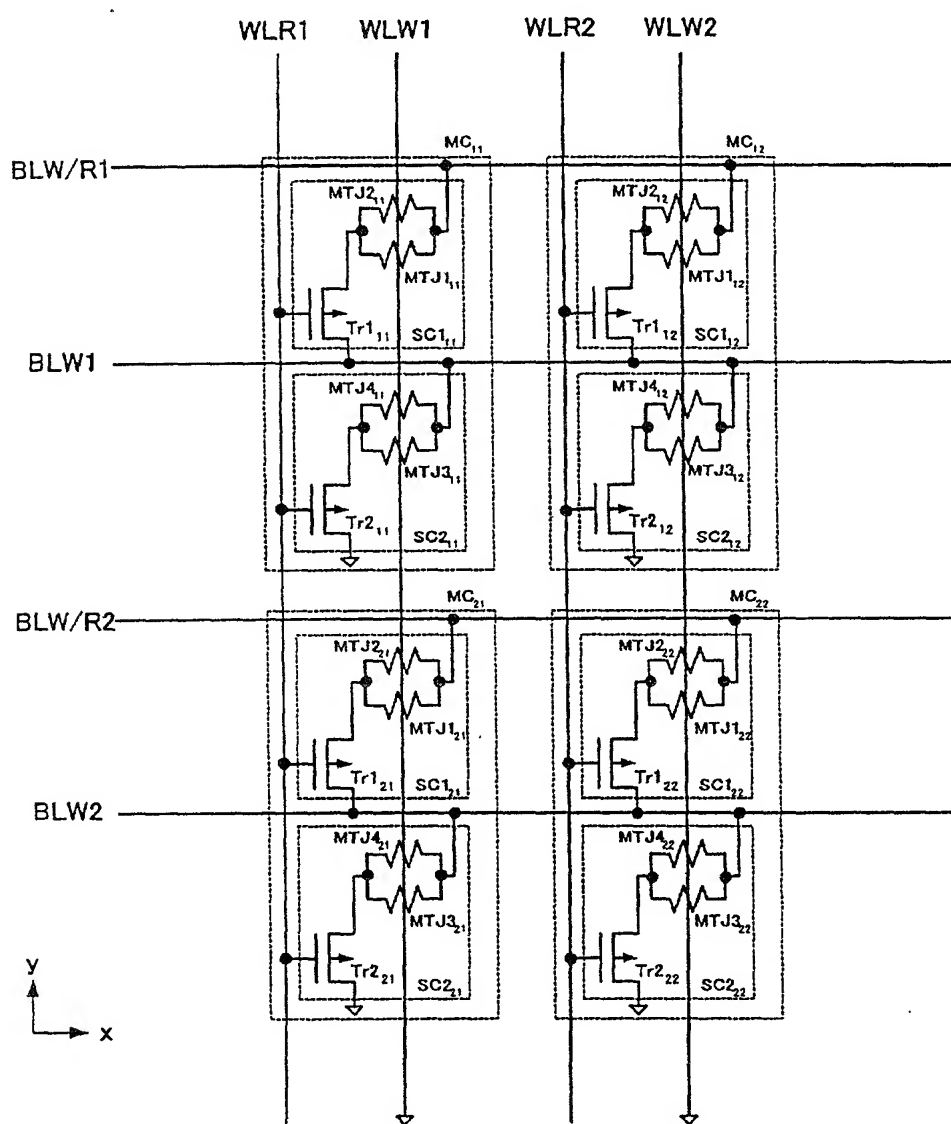


Figure 2a is a plan view of a semiconductor device. The device is divided into two main horizontal sections, BLW/R (top) and BLW (bottom), separated by a central region 11. Each horizontal section contains a central area with four memory cells (MTJ1, MTJ2, MTJ3, MTJ4) and two peripheral areas (6-1, 6-2). The memory cells are arranged in a 2x2 grid. The peripheral areas contain transistors (Tr1, Tr2) and sense amplifiers (SC1, SC2). The device is bounded by a word line (WLW) and a bit line (BLW). A coordinate system (x, y) is shown at the bottom left.

[illegible]

Figure 3

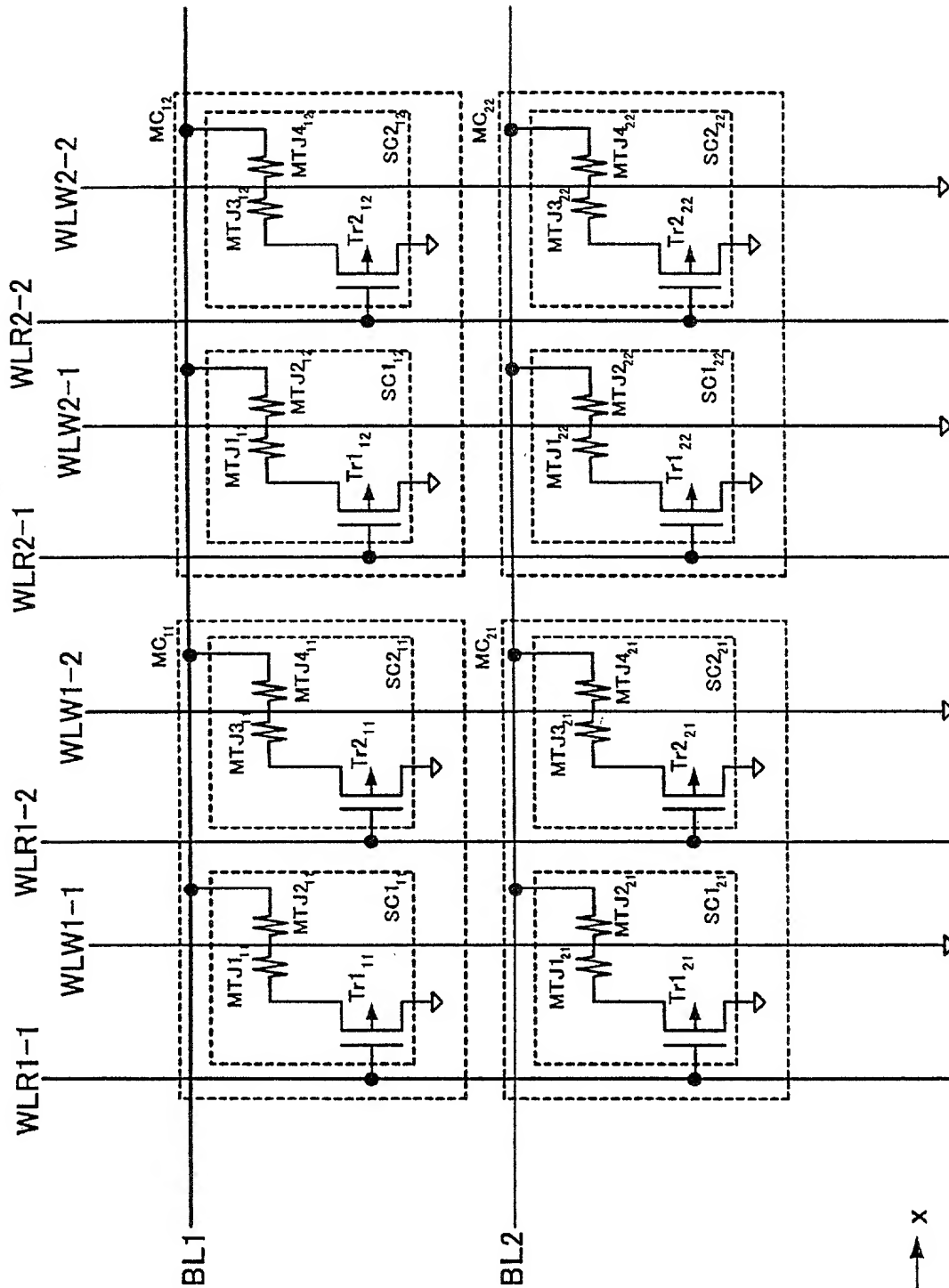


Figure 4

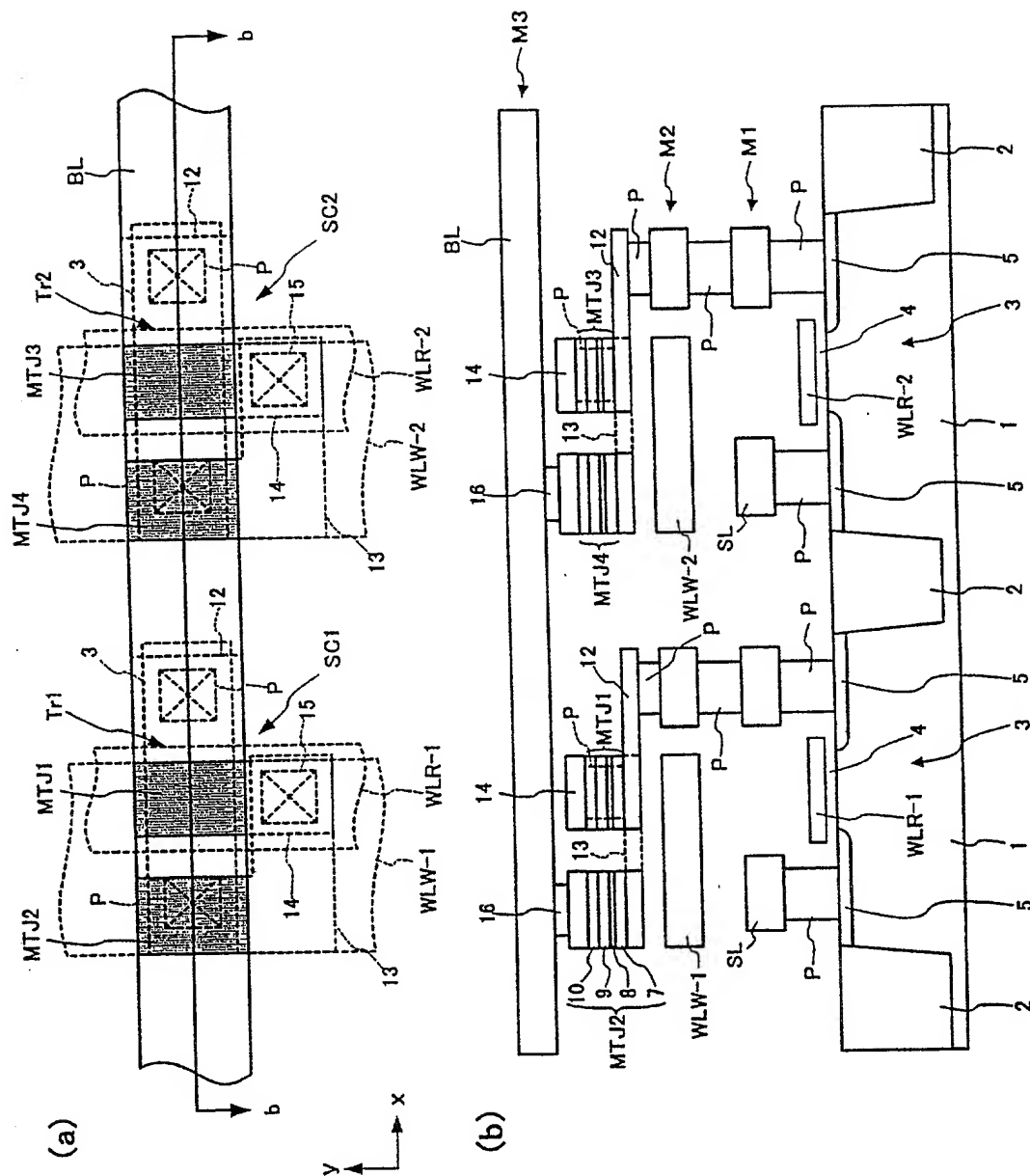


Figure 5

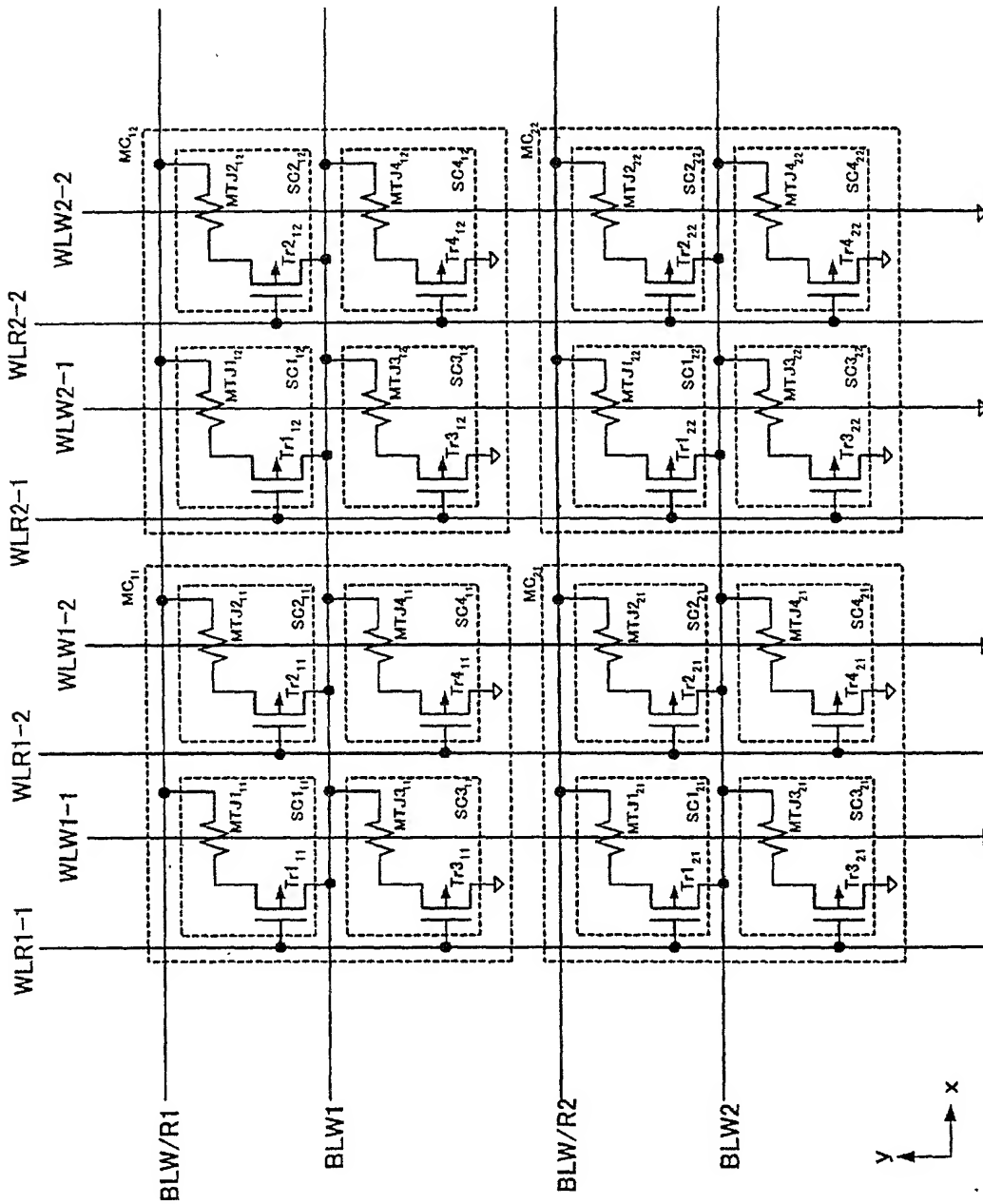


Figure 6

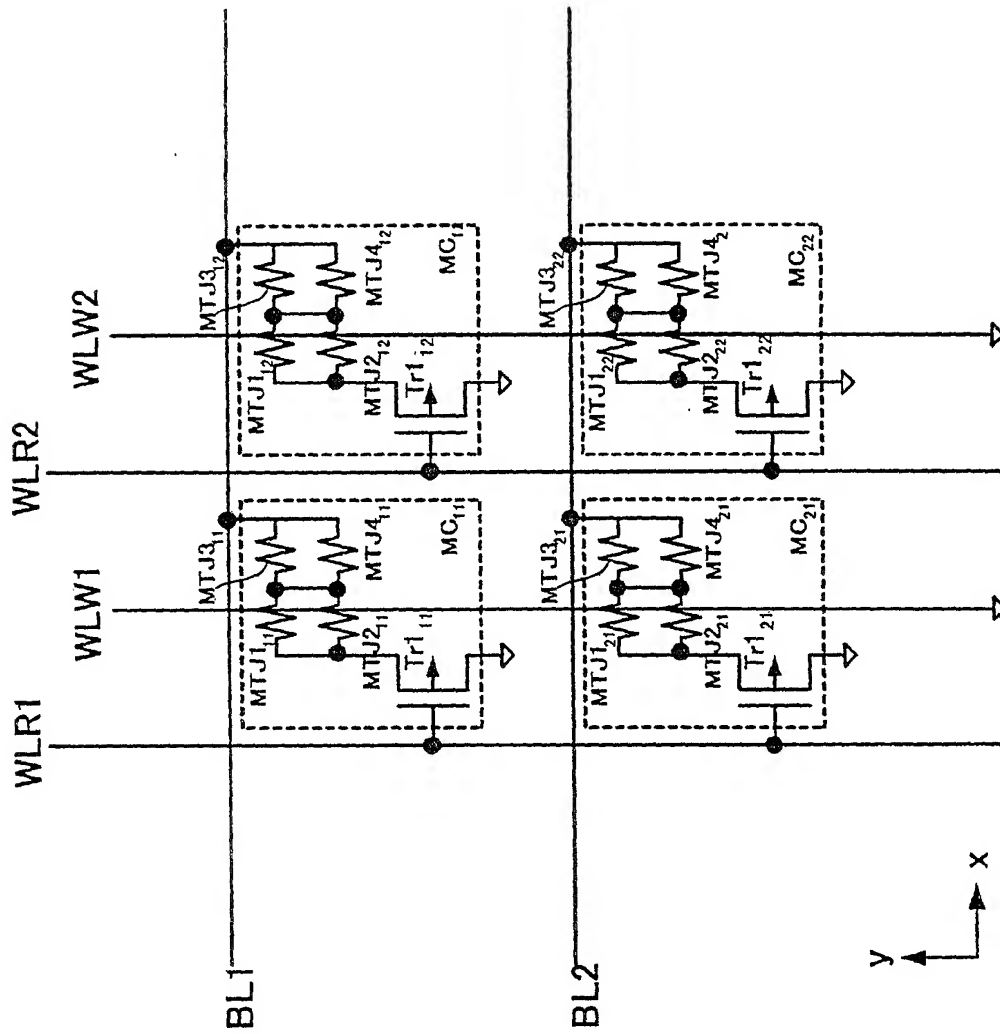


Figure 7

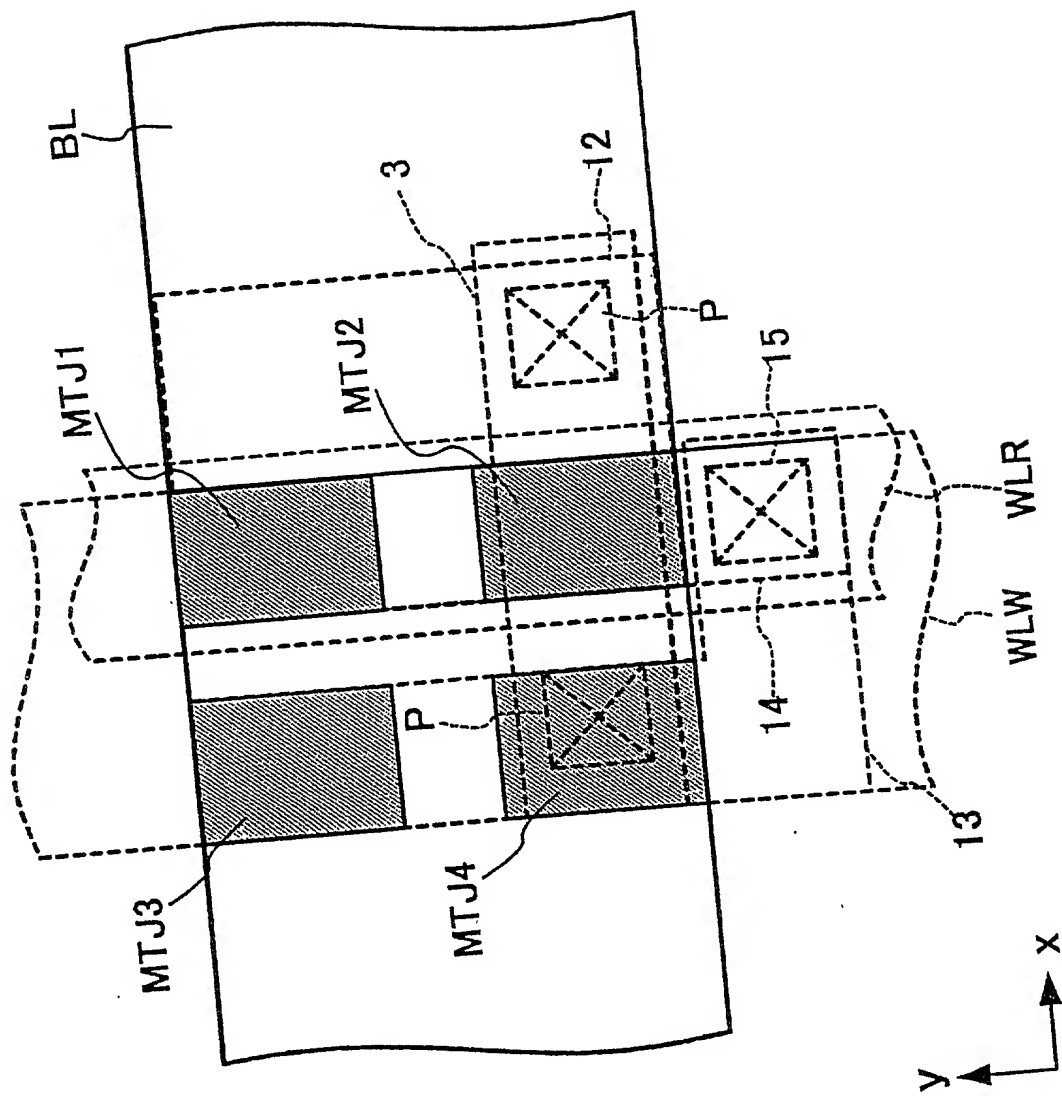


Figure 8

